METHOD AND APPARATUS FOR MANAGING POWER CONSUMPTION ON A BUS

TECHNICAL FIELD OF THE INVENTION

This invention relates in general to devices which communicate through a bus, and more particularly, to techniques by which such devices report through the bus the extent to which they provide power to or draw power from the bus.

BACKGROUND OF THE INVENTION

Various industry-standard protocols have been developed to facilitate communication between computers and peripherals. In most of these arrangements, multiple devices are coupled to and communicate through some form of bus, which may be one central bus to which all items are coupled, multiple bus sections coupled in a daisy-chain configuration, or some other arrangement. Some of these standards permit a device to draw some or all of its operating power from the bus under certain conditions.

One example is the IEEE 1394 communication protocol, promulgated by the Institute of Electrical and Electronic Engineers. This standard categorizes devices according to the manner in which they handle operating power. In this regard, some devices generate all of their own operating power, plus some excess power which they supply to the bus. Other devices generate their own operating power, but do not supply any excess power to the bus. Still other devices draw some or all of their operating power from the bus.

With respect to this latter type of device, the IEEE 1394 standard permits each such device to draw up to 3 watts of operating power from the bus. If the device needs additional operating power, it must first submit a request for additional power across the bus while drawing no more than 3 watts, and must specify how much additional power it wants. A bus master which manages the bus will then determine if there are other devices on the bus that are generating sufficient excess power to meet the need of the requesting device. If so, then the requesting device will be granted authorization to draw

that additional power from the bus. Otherwise, the requesting device will be denied authorization to draw additional power from the bus, and will typically not become fully operational.

When each device is powered up, or when a reset occurs on the bus, the device reports to the bus master which of several categories it falls in with respect to use of bus power, so that the bus master knows whether some devices are supplying excess power to the bus which other devices can be authorized to utilize, and knows the extent to which some devices are drawing the excess power from the bus. In this regard, each device typically knows it is permanently allocated to a single predetermined power utilization category, reflecting how it was designed to operate.

While existing approaches of this type have been generally adequate for their intended purposes, they have not been satisfactory in all respects. As one example, and as noted above, if a device requests additional power from the bus but it is not available, the device will typically not become fully operational. This can annoy the user, and create dissatisfaction with the manufacturer of the device.

SUMMARY OF THE INVENTION

From the foregoing, it may be appreciated that a need has arisen for a method and apparatus which facilitate operation of a device that is capable of drawing its operational power from a bus. According to the present invention, a method and apparatus are provided to address this need, and relate to operation of a device having a first coupling section which can detachably couple the device to a bus that includes a power line, having a second coupling section which can detachably couple the device to a source of power, and having circuitry coupled to each of the first and second coupling sections. The method and apparatus involve: operating the circuitry in a selected one of a plurality of modes, including a first mode in which the circuitry draws operating power from the power line through the first coupling section when no power is being received through the second coupling section, and a second mode in which the circuitry draws power through the second coupling section when a power source is supplying power to the second coupling section; automatically determining which of the first and second modes the circuitry is currently operating in; and automatically reporting through the first coupling section which of the first and second modes the circuitry is currently operating in.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the present invention will be realized from the detailed description which follows, taken in conjunction with the accompanying drawings, in which:

FIGURE 1 is a diagrammatic perspective view of an information storage device which embodies aspects of the present invention; and

FIGURE 2 is a block diagram of the information storage device of FIGURE 1, showing selected internal components of the information storage device.

DETAILED DESCRIPTION OF THE INVENTION

FIGURE 1 is a diagrammatic perspective view of an information storage device 10 which embodies aspects of the present invention, and which can be coupled by a cable 12 to a not-illustrated computer system of a known type. The information storage device 10 includes a receiving unit or cradle 13, and includes an information storage cartridge 14 which is removably inserted into the cradle 13. The cartridge 14 is inserted into and removed from the cradle 13 in directions which are approximately vertical, as indicated by a double-headed arrow 16 in FIGURE 1. In the disclosed embodiment, communications through the cable 12 are carried out according to a industry-standard protocol commonly known as IEEE 1394, which was promulgated by the Institute of Electrical and Electronic Engineers, and which is often referred to by the alternative name of "FireWire".

The cradle 13 includes a base or interface module 17, and a drive module 18. The interface module 17 and drive module 18 are physically separate modules, and are releasably coupled to each other by a not-illustrated coupling mechanism. Details of the coupling mechanism are not needed in order to understand the present invention, and the coupling mechanism is therefore not illustrated and described here in detail. Two manually operable release buttons are provided on opposite sides of the drive module 18, and one of these two buttons is visible at 22 in FIGURE 1. When the two release buttons 22 are simultaneously manually pressed, the detachable coupling between the drive module 18 and the interface module 17 is released, so that these modules can be separated.

The interface module 17 has a window 23 provided through a front wall portion thereof. A liquid crystal display (LCD) 26 is provided on the drive module 18, and is visible through the window 23 of the interface module 17 when these two modules are releasably coupled together. A manually operable eject button 27 is provided on the interface module 17. When the eject button 27 is manually pressed downwardly, the interface module 17 sends the drive module 18 an electrical signal, and this signal causes the drive module 18 to release a locking or latching mechanism that releasably holds the cartridge 14 in place, and to then effect a partial ejection of the cartridge 14. Details of this mechanism are not needed in order to understand the present invention, and this mechanism is therefore not illustrated and described in detail.

The device 10 is capable of operating in two different modes. In one mode, the device 10 draws its operating power from the IEEE 1394 bus which extends through the cable 12. In the second mode, an external power source 31 of a known type is coupled through a cable 32 to the device 10. When the external power source 31 is coupled to the device 10 through the cable 32, the device 10 draws all of its operating power from the external power source 31, and draws little or no operating power from the bus in cable 12.

With respect to the first mode of operation, in which the device 10 draws power from the bus, the industry-standard specification for the IEEE 1394 protocol specifies that any device coupled to the bus may unconditionally draw a limited amount of operating power from the bus in cable 12, which should not exceed 3

watts. If a device wants to draw more power from the bus, it must send a request to do so through the cable 12, using no more than the allowable 3 watts to make the request. The request must specify the amount of additional power that the device is seeking, indicating either that it wants up to 3 additional watts of power, or up to 7 additional watts of power. In the disclosed embodiment, the device 10 is designed to submit such a request, to seek permission to draw an additional 7 watts from the bus, or in other words a total 10 watts.

The decision of whether to grant authorization to a device to draw additional power is made on the basis of how many devices are currently coupled to the bus, and the extent to which unused power is or is not currently available on the bus. If sufficient unused power is currently available, then the requesting device will be sent a "LinkOn" command through the cable 12, according to the industry-standard protocol. In response to the LinkOn command, the device will begin drawing additional power from the bus. If excess power is not available, the LinkOn command will not be not transmitted to the device. The device will therefore not draw the extra power it wants from the bus, therefore will not enter a fully operational status, and thus will usually not attempt further interaction with the bus.

In order to facilitate evaluation of how much excess power is available on the bus at any given point in time, each device is required to report how it interacts with the bus with respect to the use of power. In this regard, according to the industry-standard specification, each device coupled to the IEEE 1394 bus is required to report the manner in which it uses bus power when it is

first powered up, when the IEEE 1394 bus is subjected to a reset, and/or when it detects that it has been coupled to the bus.

Some devices generate all of the power that they need for their own operation, and also generate some excess power which they supply to the bus, for example in quantities of at least 15 watts, at least 30 watts, or at least 45 watts. Other devices generate the power that they need for their own operation, but do not supply any excess power to the bus. Still other devices, as discussed above, draw some or all of their operating power from the bus, in amounts of 3 watts or less, 6 watts or less, or 10 watts or less. As noted above, these latter devices are each permitted to initially draw only 3 watts from the bus, but must request and then be granted authorization to draw a specified amount of additional power from the bus. According to the industry-standard specification, these various types of devices are classified into seven or eight categories, which are set forth in Table 1.

TABLE 1 - IEEE 1394 POWER UTILIZATION CATEGORIES

Category	Binary Code	Description
0	000	Device does not need power and does not repeat power.
1	001	Device is self-powered and provides a minimum of 15 W to the bus.
2	010	Device is self-powered and provides a minimum of 30 W to the bus.
3	011	Device is self-powered and provides a minimum of 45 W to the bus.

4	100	Device may be powered by the bus, using no more than 3 W. No additional power is needed to enable the link.
5	101	Reserved for future standardization.
6	110	Device is powered from the bus, and using no more than 3 W. An additional 3 W is needed to enable the link.
7	111	Device is powered from the bus, and using no more than 3 W. An additional 7 W is needed to enable the link.

From the foregoing discussion, it should be evident that the disclosed device 10 of FIGURE 1 operates in category 7 (binary code 111) if the external power source 31 is not present, and operates in category 4 (100) if the external power source 31 is present. As discussed above, devices are required to report how they interact with the bus in regard to power use, and they make this report by sending a packet which includes the appropriate binary code from Table 1. A report which includes either of the binary codes "110" and "111" also inherently constitutes a request for permission to draw additional power from the bus.

FIGURE 2 is a block diagram of the information storage device of FIGURE 1, showing selected internal components. FIGURE 2 is not intended to show all of the internal components of the device 10, but only components that help to convey an understanding of the present invention. As shown in FIGURE 2, the cartridge 14 has a connector 41, and the drive module 18 has a connector 42 which releasably engages the connector 41 when the cartridge 14 is removably disposed in the drive module

18. The cartridge 14 contains a hard disk drive mechanism 56. The internal structure of the hard disk drive mechanism is known, and detailed information about that internal structure is not needed in order to understand the present invention. Accordingly, the internal structure of the hard disk drive mechanism 56 is not illustrated in the drawings, and is only briefly discussed here for purposes of completeness.

In particular, the hard disk mechanism 56 includes a sealed housing, and includes within the sealed housing a data storage medium in the form of a rotatable hard disk having a magnetic material on one side thereof, and a spin motor which can effect rotation of the hard disk. The hard disk drive mechanism 56 also includes within the sealed housing an actuator arm supported for pivotal movement, a read/write head supported at one end of the actuator arm for movement adjacent and approximately radially of the magnetic surface on the disk in response to pivotal movement of the arm, and a voice coil motor (VCM) which effects pivotal movement of the actuator arm in response to electrical signals.

The drive module 18 includes a drive circuit 71, which is coupled to the hard disk drive mechanism 56 through a bus that includes portions 72 and 73 respectively disposed in the drive module and the cartridge. The connectors 41 and 42 electrically couple the portions 72 and 73 of the bus when the connectors are matingly engaged. The drive circuit 71 controls the LCD 26. The drive circuit 71 has internal structure of a known type, and detailed information about that internal structure is not needed in order to understand the present invention. Accordingly, the internal structure

of the drive circuit 71 is not illustrated and described here in detail.

The drive module 18 has a connector 81, and the interface module 17 has a connector 82 which releasably engages the connector 81 when the drive module 18 is releasably coupled to the drive module 17 in the configuration shown in FIGURE 1. The interface module 17 includes a bridge circuit 86, which is coupled to the drive circuit 71 in the drive module 18 by an AT Attachment (ATA) bus that has portions 87 and 88. When the connectors 81 and 82 are matingly engaged, they electrically couple the bus portion 87 to the bus portion 88. The ATA bus 87-88 conforms to an industry-standard specification, which is well known to those skilled in the art.

In the disclosed embodiment, the bridge circuit 86 is an integrated circuit which is commercially available as part number TSB42AA9 from Texas Instruments Incorporated of Dallas, Texas. The bridge circuit 86 includes a processor 91, which executes a firmware program that is stored in a read only memory (ROM) 92. The bridge circuit 86 is coupled through a bus 93 to a circuit 95, which is commonly referred to in the industry as a PHY circuit. In the disclosed embodiment, the PHY circuit 95 is an integrated circuit commercially available as part number TSB41AB2 from Texas Instruments Incorporated.

The interface module 17 has a connector 101, which can matingly engage a connector 102 provided at the end of the cable 12, so that the cable 12 can be selectively disengaged from the interface module 17 by separating the connectors 101 and 102. When the connectors 101 and 102

are engaged, a subset of the lines within the cable 12 are coupled through the connectors 101-102 and a bus 103 to the PHY circuit 95. A further line within the cable 12, which carries operating power, is coupled through the connectors 101-102 to a cable power line 104 disposed within the interface module 17.

The interface module 17 includes a further connector 111. The connector 111 can be matingly engaged by a connector 112 provided at the end of a cable 113, the other end of the cable 113 being coupled to a device 116. The device 116, the cable 13 and connector 112 are optional, and are therefore shown in broken lines in FIGURE 2. Communications through the cable 113 are effected according to the IEEE 1394 protocol. When the device 116 is present, a subset of the lines within the cable 113 are coupled through a bus 117 to the PHY circuit 95. A further line within the cable 113 is coupled to the cable power line 104 in the interface module 17. The PHY circuit 95 operatively couples the device 116 to the IEEE 1394 bus within the cable 12. Thus, when the device 116 is present, it is effectively daisy-chained to the device 10, which in turn is daisy-chained through the cable 12 to some other device on the IEEE 1394 bus.

The interface module 17 has a further connector 121, which can matingly engage a connector 122 provided at the end of the cable 32 for the external power source 31. When the connectors 121 and 122 are matingly engaged, direct current (DC) power is supplied through a line in the cable 32 to an external power line 123 located within the interface module 17.

A DC-TO-DC converter circuit 141 is provided within the interface module 17, and in the disclosed embodiment is a component commercially available as part number LM2672 from National Semiconductor of Santa Clara, California. In the interface module 17, the DC-TO-DC converter circuit 141 serves as a voltage regulator, and receives an input voltage from the cable power line 104. The output of the converter circuit 141 is coupled to a line 142, which provides operating power (VCC) to other components within the information storage device 10.

The external power line 123 is coupled to a disable input of the converter circuit 141, is also coupled to ground through a resistor 146, and is coupled to the anode of a diode 147. The cathode of the diode 147 is coupled to the VCC line 142. The external power line 123 is also coupled through a further resistor 151 to the base of a bipolar junction transistor 152, the emitter of which is coupled to the ground. The collector of the transistor 152 is coupled through a resistor 153 to the DC operational voltage VCC.

The PHY circuit 95 has three inputs A, B and C. In pre-existing systems, these three inputs are each permanently hardwired to a logic high or a logic low. In the disclosed embodiment of FIGURE 2, however, the input A is coupled to operating power VCC, but the inputs B and C are each coupled to the collector of transistor 152. The inputs A, B and C permit a three-bit binary code to be introduced into the PHY circuit 95, where input A is the most significant bit, and input C is the least significant bit. This three-bit binary code corresponds to the middle column of Table 1, as discussed later.

A reset circuit 161 of a known type has an input which is coupled to and monitors the VCC line 142, and has an output coupled to reset inputs of the PHY circuit 95 and the bridge circuit 86. The output of the reset circuit 161 is also coupled through the connectors 81 and 82 to the drive circuit 71. When the voltage on line 142 is below a predetermined threshold level, the reset circuit 161 applies a reset signal through its output 162 to each of the components coupled to the line 162. Thus, at power up, the reset circuit 161 outputs the reset signal on line 162 until operating power on the VCC line 142 is above the threshold level, and then terminates the reset signal on line 162 so that components within the information storage device 10 can commence normal operation. If operating power on VCC line 142 should happen to drop below the threshold level during normal operation, the reset circuit 161 will detect this and generate a system reset on line 162, in order to reset each device coupled to line 162 and thereby prevent operational errors until operating power on line 142 is again above the threshold level, at which time the system reset signal is terminated.

The interface module 17 includes an eject switch 171, which is operated by the eject button 27. The eject switch 171 has an output which is coupled to the drive circuit 71 through the connectors 81-82.

The operation of the system 10, and in particular the interface module 17, will now be briefly discussed. Assume that the external power source 31 is not currently present, or in other words that connector 122 is not engaged with connector 121. The resistor 146 and resistor 151 form a voltage divider which hold the

external power line 123 at a voltage which is low enough to enable the converter circuit 141. Consequently, power received through cable 12 (and also possibly cable 13) is supplied through the cable power line 104 to the main input of the converter circuit 141. The converter circuit 141 processes and regulates this DC voltage, and produces the DC operating power VCC at its output on line 142.

The reset circuit 161 will initially be keeping appropriate components within the information storage device 10 in a reset mode. But once the operating voltage VCC on line 142 exceeds a predetermined threshold, the reset circuit 161 will terminate the reset signal on its output line 162, thereby permitting the device 10 to commence normal operation.

After the reset signal has been removed from the PHY circuit 95, the PHY circuit reads the three-bit binary word present at its inputs A, B and C. Since input A is coupled to VCC, it will always be a logic 1. When the external power source 31 is not present or is not active, the external power source 31 will not be applying any voltage to line 123. Thus, the resistor 153, the base-collector junction of transistor 152, and the resistors 151 and 146 will form a voltage divider which causes the disable input of the converter circuit 141 to be coupled through a low impedance to ground. Consequently, the converter circuit 141 will be enabled, and will be produce regulated DC operating power at its output on the VCC line 142.

The voltage on line 123 will be lower than the voltage on line 142. As a result, no current will be passing through the diode 147. Due to the diode 147, no

base current will be flowing into transistor 152, and thus transistor 152 will be off. Consequently, there will be little or no current flowing through the resistor 153, and the voltage across it will be approximately zero volts. Thus, each of the three inputs A, B and C of the PHY circuit 95 will be receiving a logic 1, representing the binary code "111". As discussed above, this corresponds to category 7 in TABLE 1.

Shortly after the reset circuit 161 ends the power-on system reset on line 162, the circuitry within the PHY circuit 95 will read the three-bit code from its inputs A, B and C, and then report this code through the bus 12 to a bus master at a remote location, in accord with the IEEE 1394 protocol. This binary code indicates that the information storage device 10 of FIGURE 2 is drawing power from the IEEE 1394 bus in an amount of 3 watts or less, but wishes to draw up to 7 additional watts from the bus. If the bus master determines that there is sufficient excess power for the information storage device 10 to receive the 7 additional watts requested, then the bus master will send through the cable 12 a LinkOn command, in response to which the information storage device 10 will begin drawing more power from the bus 12, and will commence normal operation. Thereafter, the PHY circuit 95 ignores the inputs A, B and C during normal operation.

On the other hand, if the bus master determines that there is not enough excess power for the information storage device 10 to receive the 7 additional watts it requested, then the device 10 might be precluded from operating if it had to rely on power from the IEEE 1394 bus. However, it will be recognized that the present

invention allows a user to elect to attach the external power source 31 to the device 10 and thus make the device 10 operational even though there is not currently enough excess power on the bus to meet the needs of the device.

Assume now that the connector 122 is manually coupled to the connector 121, in order to couple the external power source 31 to the interface module 17. The external power source 31 will thus be supplying external power to the line 123 in the form of a DC voltage. The application of this DC voltage to the disable input of the converter circuit 141 will disable the circuit 141, so that it ignores the power available on the cable power line 104 from the cable 12 and/or the cable 113.

The voltage present on line 123 will be high enough so that current can flow through the diode 147 and establish the appropriate operating voltage on VCC line 142. Further, the voltage on line 123 acts through resistor 151 to produce at the base of transistor 152 a voltage sufficient to turn on the transistor 152. Consequently, current will flow through the resistor 153, creating a voltage across the resistor which causes the inputs B and C of the PHY circuit 95 to each appear to the PHY circuit to be a logic low. Therefore, the binary code "100" will be present and waiting at inputs A, B and C of the PHY circuit 95.

When the reset circuit detects that the operating power VCC on line 142 is above the required threshold, it terminates the reset signal on line 162, and then the PHY circuit 95 will in due course read the three-bit category code "100" which is waiting at its inputs A, B and C. The PHY circuit then automatically forwards this binary code through the cable 12 to a bus master, as discussed

above. This code corresponds to category 4 in Table 1. Thereafter, normal operation of the information storage device 10 commences, and the PHY circuit 95 ignores its inputs A, B and C during normal operation.

Assume that, while the information storage device 10 is operating as a category 4 device under power from the external power source 31, a user inadvertently or intentionally disengages the connector 122 from the connector 121. The loss of external power on line 123 will enable the converter circuit 141, so that it takes power from cable power line 104, and in due course begins producing operating power on the VCC line 142. However, it takes a short but finite time interval for the converter circuit 141 to transition from its disabled state to its enabled state, which in the disclosed embodiment is approximately 100 milliseconds.

During this time interval, the power which the reset circuit 161 receives on line 142 from the external power line 123 through the diode 147 will drop somewhat, to a level below the threshold. This will cause the reset circuit 162 to output onto line 162 a system reset. Once the converter circuit 141 has completed the transition from its disabled state to its enabled state, it will be producing power on the VCC line 142 which is above the threshold and which thus causes the reset circuit 161 to terminate the system reset signal that it generated. Consequently, the information storage device 10 will again commence the initialization process that leads to normal operation.

As part of this, the PHY circuit 95 will read its inputs A, B and C, and forward this three-bit binary word to the remote bus master. At this time, the three-bit

binary word will be the code "111", indicating that the device 10 is now operating as a category 7 device drawing 3 watts or less from the IEEE 1394 bus, but wants to draw up to 7 watts of additional power from the bus. In this manner, due to the reset from reset circuit 161, the interface storage device 10 will again log onto the IEEE 1394 bus, in a manner similar to that described above for the case where power is turned on. If the bus master determines that there is sufficient excess power available on the bus to meet the request of the device 10, the bus master will send a LinkOn command that authorizes the information storage device 10 to begin drawing additional power through the cable 12. Thus, in the event that power from the external power source 31 is lost in the middle of normal system operation, a smooth transition will occur from operation on power from the source 31 to operation on power from the cable 12, in conjunction with reporting across the bus that the system is now operating in category 7 rather than category 4.

The foregoing discussion of FIGURE 2 is directed to one embodiment of the present invention. Still referring to FIGURE 2, an alternative embodiment is almost the same, except that the external power line 123 has an additional section represented by broken line 201, which extends to an input of the bridge circuit 86. It will be recognized that, in this alternative embodiment, the bridge circuit can sense the state of the external power line 123, and thus determine whether or not the device 10 is currently receiving power from the external power source 31. The bridge circuit periodically polls the state of the line 123 (through the portion 201 thereof). In the disclosed embodiment, the bridge circuit has an

interrupt input driven by a crystal oscillator so as to produce interrupts at periodic intervals such as every 10 milliseconds, in order to facilitate timekeeping functions within the program executed by the bridge circuit. The line 123 is polled by the interrupt service routine each time the oscillator interrupt occurs.

One other difference, not visible in FIGURE 2, is that the threshold of the reset circuit 161 is set to be somewhat lower. As a result, when the external power source 31 is disengaged from the device 10 while the device 10 is carrying out normal operation as a category 4 device, the reset circuit 161 will not generate a reset during the time required for the converter circuit to 141 to transition from its disabled state to its enabled state.

In this alternative embodiment, operation at power up is effected in substantially the same manner already discussed above. On the other hand, when the connectors 121 and 122 are engaged or disengaged during normal operation of the device 10, the sequence of events is somewhat different.

In this regard, assume that the information storage device 10 is currently operating on power from the external power source 31. Assume also that the connectors 121 and 122 are suddenly disengaged, either inadvertently or intentionally. This will cause the voltage on line 123 to drop, such that in due course the bridge circuit 86 will poll this line and determine that it has changed from a logic high to a logic low. This change tells the bridge circuit that the device 10 is no longer receiving operating power from the external power source 31. The bridge circuit 86 responds by instructing

the PHY circuit 95 to effect a reset operation on the IEEE 1394 bus, and this reset operation will in turn force all devices on the bus, including the device 10, to pursue essentially the same techniques used to gain access to the bus at power up, and to report the power consumption category in which they are operating.

It will be recognized that, at this time, the inputs A, B and C to the PHY circuit 95 will be carrying the three-bit binary code 111, causing the PHY circuit to advise the bus master that the information storage device 10 is currently operating in category 7, or in other words using 3 watts from cable power line 104 while requesting permission to draw additional power. This request is authorized where possible, in the manner already described above.

As a different scenario, assume that the information storage device 10 is operating under power from the IEEE 1394 interface on bus 12, and that a user intentionally engages the connector 122 with the connector 121, in order to couple the external power source 31 to the information storage device 10. The power source 31 will promptly provide DC power to line 123 and, through diode 147, to VCC line 142. The voltage on line 123 will disable the converter circuit 141, so that very shortly thereafter it stops trying to supply power to line 142. Since line 123 (including portion 201 thereof) will have transitioned from a logic low voltage to a logic high voltage, the bridge circuit 86 will detect this change the next time it polls the input coupled to line 123, and will then cause the PHY circuit 95 to effect a reset of the IEEE 1394 bus. As before, this reset causes the PHY circuit 95 to read its three inputs A, B and C in the

same manner discussed above in association with a power-up condition, and to use this three-bit code, which is a binary 100, to report to the bus master its current power status, which is category 4.

The present invention provides a number of technical advantages. One such technical advantage is that, in the context of an IEEE 1394 environment, a device can be selectively operated in either of two modes, where power is respectively obtained from either the IEEE 1394 bus or an external power source. According to a related advantage, the device can automatically determine at power-up its current source of operating power, and then report this information to a remote bus master which manages the bus.

According to another advantage, the device can automatically handle disconnection of the external power source during system operation, including reporting to the bus master of the change in its power consumption category. A similar advantage is that the device can automatically handle connection of the external power source during system operation, including reporting to the bus master of the change in its power consumption category.

According to another advantage, the device includes a processor which has the capability to monitor at least one source of operating power and automatically detect any change in the source of operating power, and then ensure that the change in its source of operating power is reported to the bus master. According to a related advantage, the processor can cause the reporting to occur by initiating a reset operation on the IEEE 1394 bus.

Although two embodiments have been illustrated and described in detail, it will be understood that various substitutions and alterations can be made therein without departing from the spirit and scope of the present invention, as defined by the following claims.